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13. ABSTRACT (Maximum 200 words) <p>Photodetection circuits form the first stage of the artificial image acquisition process. The image acquisition circuits discussed in this final report pertain to circuits fabricated in a standard CMOS process. Such circuits offer advantages such as random access to a pixel, faster readout, integration of processing circuitry on the same die, low voltage and low power dissipation, and lower cost over the conventional Charge Coupled Device (CCD) process.</p> <p>We describe a new locally adaptive multimode photodetector circuit. The advantages of the circuit are local adaptation, wide dynamic range, excellent sensitivity, and large output voltage swing. The circuit was fabricated in the 2 CMOS process through MOSIS. Simulation and experimental results of the circuit are given.</p> <p>The research contract generated 12 papers and supported 7 graduate students.</p>				
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# **Locally Interconnected Adaptable Architectures**

**Lex A. Akers, Arizona State University**

## **Final Report**

**Grant No N00014-96-1-0107**

### **Summary**

Photodetection circuits form the first stage of the artificial image acquisition process. The image acquisition circuits discussed in this final report pertain to circuits fabricated in a standard CMOS process. Such circuits offers advantages such as random access to a pixel, faster readout, integration of processing circuitry on the same die, low voltage and low power dissipation, and lower cost over the conventional Charge Coupled Device (CCD) process.

We describe a new locally adaptive multimode photodetector circuit. The advantages of the circuit are local adaptation, wide dynamic range, excellent sensitivity, and large output voltage swing. The circuit was fabricated in the  $2\mu$  CMOS process through MOSIS. Simulation and experimental results of the circuit are given.

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### **I. Introduction**

Human vision is an image capture and processing system of enormous complexity comprising the retina, visual cortex, and other interconnected brain systems. It is believed that over 55% of the human cortex is devoted to vision processing. The building of such a system artificially is truly a big challenge. The first step in such a system is the transduction of light into electrons. The circuits used for image acquisition are called photodetection circuits or image sensors. Signals from the photodetector circuits are either directly stored in memory or further processed and stored. The stored data is used to reconstruct the captured image, for example on a computer screen or further processing is done to extract the information contained in the image.

The basic technologies used for image acquisition are CCD imagers, and CMOS imagers. While the CCD technology has been dominant till now, CMOS technology offers advantages such as random access to a pixel, faster readout, integration of processing circuitry on the same die, low voltage and low power dissipation, and lower cost over the conventional Charge Coupled Device (CCD) process.

Charge coupled devices are special semiconductor devices, fabricated with specialized and costly processes, used for image acquisition. CCD's sense light intensity by integrating the photocharge in time on a grid of (for example) 860 by 640 pixels. The charge is then shifted out to a register one pixel at a time and read out is destructive. The process is exotic and costly because of the high charge transfer efficiency requirements[1]. The dynamic range of CCD is less compared to the dynamic range of light viewed by humans. When the dynamic range needed to process the image exceeds the CCD's capability, the image is clipped. Blooming can occur when the charge on a pixel exceeds its holding capacity and spills over into neighboring pixels. In a CCD camera system the photodetector array is on a separate die. The output of the CCD, normally an unconditioned analog signal, is then sent to other chips for additional processing. The output of the CCD camera is NTSC, SECAM or PAL analog output. The main drawback of a CCD process is its high cost to integrate the associated circuitry with the photodetectors on a single chip[1].

CMOS is the standard technology used in making most logic circuits. If CMOS technology is used for imaging then its cost will be less compared to a CCD. In a standard CMOS process various junction diodes, transistors and photogates can be used as photodetecting elements. The associated circuitry easily converts the charge into a voltage or current which can be randomly read from an array of pixels like a DRAM, unlike a CCD system. There are also some disadvantages. Disadvantages are fixed pattern noise, less fill factor compared to a CCD, blooming, lag, and effects of noise due to digital switching of the associated circuitry. The most popular type of photodetection circuits which include gain in the pixel are called Active Pixel Sensors (APS).

The applications for these kind of sensors are in digital cameras, multimedia applications, and in other portable vision systems. With the trend towards replacing CCD devices with CMOS, there is a demand for new and enhanced photodetecting circuits and optimum pixel architectures. These circuits are critical to a design of a CMOS imager.

We describe a new type of photodetection circuit called a Locally Adaptive Multimode Photodetector Circuit, which has a better sensitivity and increased dynamic range compared to standard photodetectors. The circuit will optimize the tradeoff between the dynamic range and sensitivity of the CMOS imagers. The operation of this kind of circuit is based on the principle of automatically adjusting the gain of the circuit such that it adapts to locally changing light intensity.

## II. Photodetection Circuits

The light intensity present in the environment varies about 14 orders of magnitude [2] with the brightest intensity corresponding to noon sunlight in June ( $1 \text{ W/cm}^2$ ) and the darkest corresponding to night sky illumination ( $10^{-14} \text{ W/cm}^2$ ). The full moon light corresponds to approximately  $10^{-6} \text{ W/cm}^2$ . The main challenge in designing a CMOS imager is to operate it over a wide dynamic range of light just like a human eye. Circuits are needed to detect light intensity over a wide range of interest which can be 7-10 decades if not the complete 14 decades. Present CMOS sensors have a dynamic range of 6-7 orders of magnitude [3], with a tradeoff between dynamic range and sensitivity. If you have large dynamic range then the sensitivity will be low and vice versa. In imaging systems which operate at 5V, the least voltage which can be detected accurately with an 8 bit A/D converter is about 20mV. Seven decades of photocurrent requires a resolution of 500nV. Gaining such a sensitivity by increasing the number of bits in an A/D is not practical since data handling would make the system complex and it is also difficult to store such small voltages on the gate capacitors so that they can be sampled at a later time.

Detecting the light intensity and converting it into an electrical parameter (voltage or current), and subsequently processing the signals from an array of detectors, in spatial and/or temporal domain, are the primary tasks of vision chips. It is very important to understand the physics behind the devices used in transduction of light as these devices play a critical role in design of photodetection circuits. The characteristics of the detectors, such as dynamic range, spectral efficiency, noise, linearity, bandwidth, etc. directly affect the performance of the system.

A *pn* junction photodiode is just a *pn* junction diode which is fabricated such that light can fall on its metallurgical junction. The absorption of light inside the diode creates electron-hole pairs. On average, minority carriers created within a diffusion length in the quasineutral regions diffuse to the depletion region. These carriers, and carriers photogenerated within the depletion region, are subsequently swept by the E-field to the opposite side of the junction, thereby contributing an added reverse current through the diode.

The junction photodiodes have a linear behavior over a dynamic range of more than 7 decades [4], with reasonable sensitivity to the visible light spectrum. In a standard CMOS process, either p-well or n-well, several parasitic junction devices are possible for photodetection. Figure 1 gives a pictorial representation of the various junction diodes possible. The first three structures are junction diodes, the fourth one is a parasitic vertical bipolar transistor, and the last structure is capable of bi-directional photocurrent generation depending on the voltage across the device. The last structure can be considered as a lateral bipolar transistor with symmetric emitter and collector which depends on the separation between the two diffusion areas. All of the photodetecting elements respond acceptably in the visual light range with slight differences depending on the depth of the junction [4].

The photodetection circuits that are most often used are:

- Logarithmic Photodetection Circuit
- Active Pixel Sensor
- Adaptive Photoreceptor Circuit
- Current mode CMOS Imager.

#### A. Logarithmic Photodetection Circuit

The characteristics of the biological photoreceptor (eye) influenced the design of the photodetector circuits. The logarithmic nature of the response of the biological photoreceptor is well supported by psychophysical and electrophysiological evidence[5]. Another important point of the logarithmic nature of the biological photoreceptor is the voltage difference between two points is proportional to the contrast ratio between the two corresponding points in the image[5]. The contrast ratio is defined as the ratio between the reflectance of two adjacent objects, reflectance which are independent of the illumination level. The logarithmic photodetector circuit is one which transduces light into a DC level which is proportional to the logarithm of the input photocurrent. Thus a wide dynamic range of light is converted into a small range of output voltage. The most common logarithmic photoreceptor circuit used is shown in Fig. 2. The simulation of the circuit shown in Fig. 3 was done in HSPICE and the models used were level 2 parameters provided by MOSIS from the Orbit 2 $\mu$  run. Simulations for different versions of this circuit were also done and the results are also shown in Fig. 3. The other versions of this circuit are just adding or subtracting load transistors. A comparison of these three circuits shows that the one MOSFET version saturates at one threshold and the three MOSFET version saturates at three thresholds. The swing for the later one is high but its sensitivity is less in the region where photocurrent is less (though not clearly seen in this graph).

There are some drawbacks for this circuit. Circuit behavior is largely dependent on the process parameters. This creates a spatial noise which is very difficult to compensate. Another drawback is its very slow response at low light intensities, which requires longer settling times. The extreme compression done to the input signal is also a big disadvantage because if an algorithm needs to differentiate between signals, the logarithmic compression reduces the chance to detect such differences, this is especially seen in circuits operating at very low contrast condition of the image. And lastly, the circuit has a low output voltage swing.

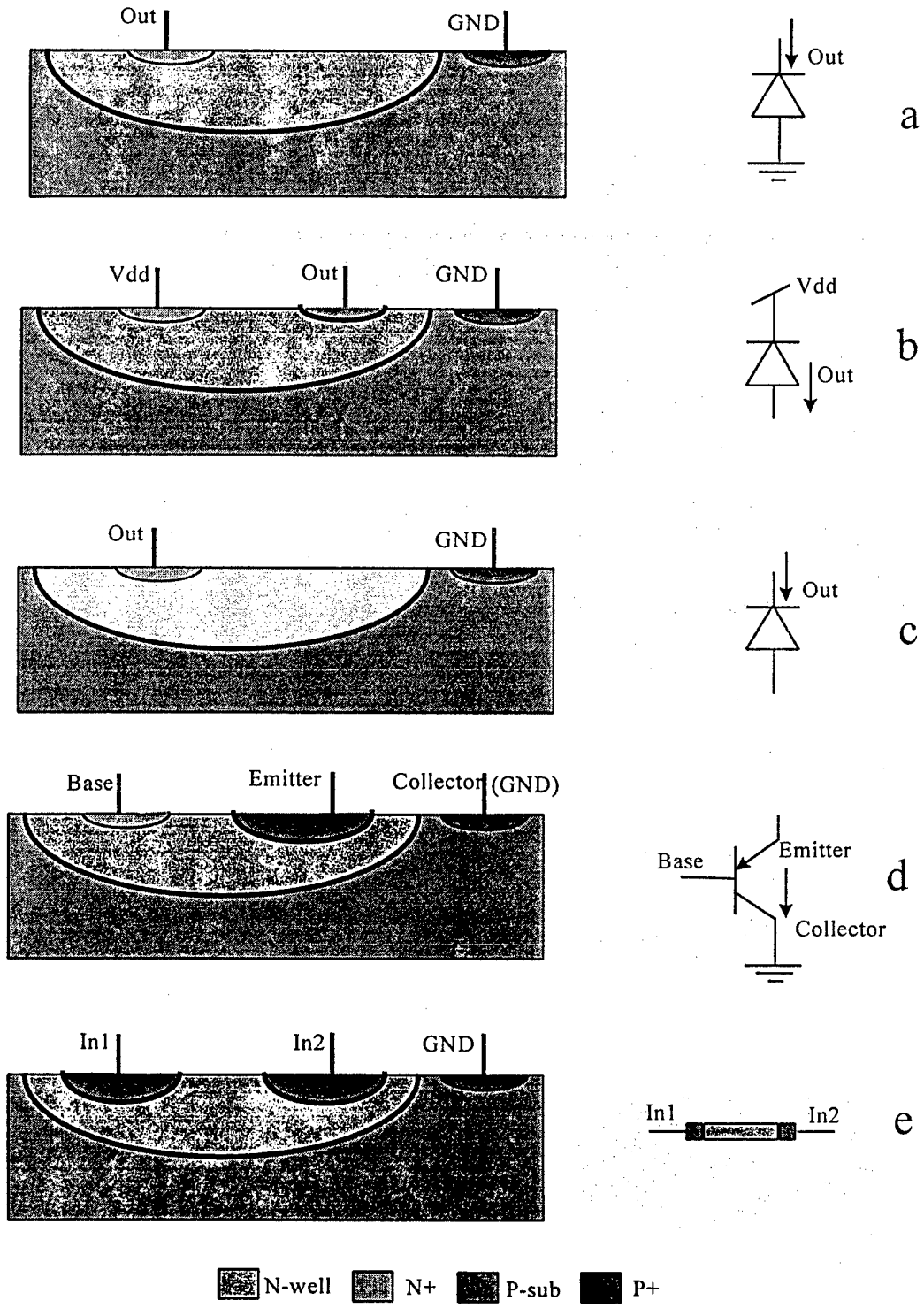


Fig 1: Photodetecting Elements Possible in CMOS Process[4].

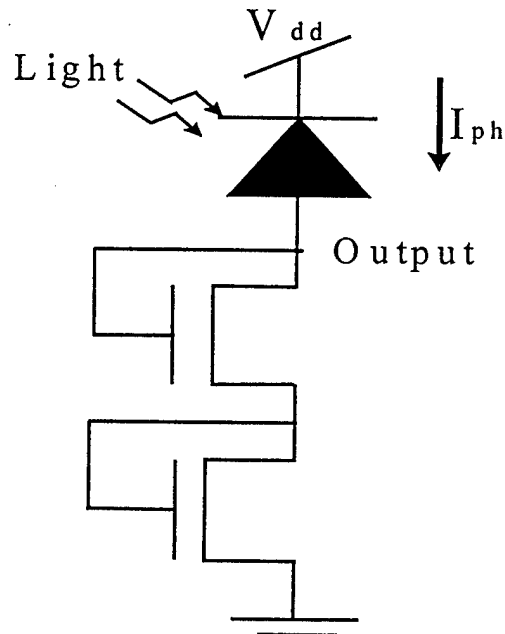


Fig. 2: Logarithmic Photoreceptor Circuit

## B. Active Pixel Sensor

A CMOS active pixel sensor (APS) is the most popular type of circuit that is used in non-CCD imaging systems. These circuits are also termed an integrating sensor. The current resulting from the photons discharges a capacitor over a fixed time period. The APS uses active transistors at each pixel site to achieve a local conversion from the charge-collection mode to the voltage-readout mode. The advantages of APS over other circuitry are electronic shuttering, variable integration time, large output swing and a dynamic range of 70-80dB[6]. A common type of APS circuit is shown in Fig. 4 and consists of a photodetecting element, a shutter, a reset transistor and two read out transistors. The read out transistors can be followed by some selection circuitry to randomly select a pixel from an array in the same manner as a DRAM cell.

The basic principle [6] of an APS involves charging the gate of a transistor in a source follower circuit, which is then discharged by a photodiode or a phototransistor. The discharge time is controlled by a shutter. The shutter speed is fixed or controlled manually depending on the intensity of light. There are different versions of APS and the standard circuit is shown in Fig. 4. Some circuits may not have the shutter transistor M2 and the discharge rate is controlled by the reset transistor M1. Some implementations have two stages of source followers for strengthening the signal and performing multiple reads [7] as shown in Fig. 5.

The circuit shown in Fig. 4 was simulated using HSPICE with level 2 parameters from the Orbit's 2 $\mu$  run. Figure 6 shows the output response for a photocurrent of 1nA. Simulations of the output voltage vs. photocurrent for a fixed shutter time of 100 $\mu$ s for the circuits of Figs. 4 and 5 are shown in Figs. 7 and 8, respectively. All these circuits were also fabricated in the 2 $\mu$  CMOS process through MOSIS and experimental measurements for the source follower APS circuit is shown in Fig. 9. The measurements were done by exposing the detector to fluorescent light and lamp light of approximately 850 lumens. The discharge rate is lower for the fluorescent light than the lamp light of higher intensity, which is expected.

The main drawback of APS is its low sensitivity. Due to the variation of the light intensity over such a wide range, the sensitivity of the circuit suffers because there is a tradeoff between sensitivity and dynamic range. The solution to this problem is adaptation. Adaptation helps in operating the circuit over a wide dynamic range with better sensitivity.

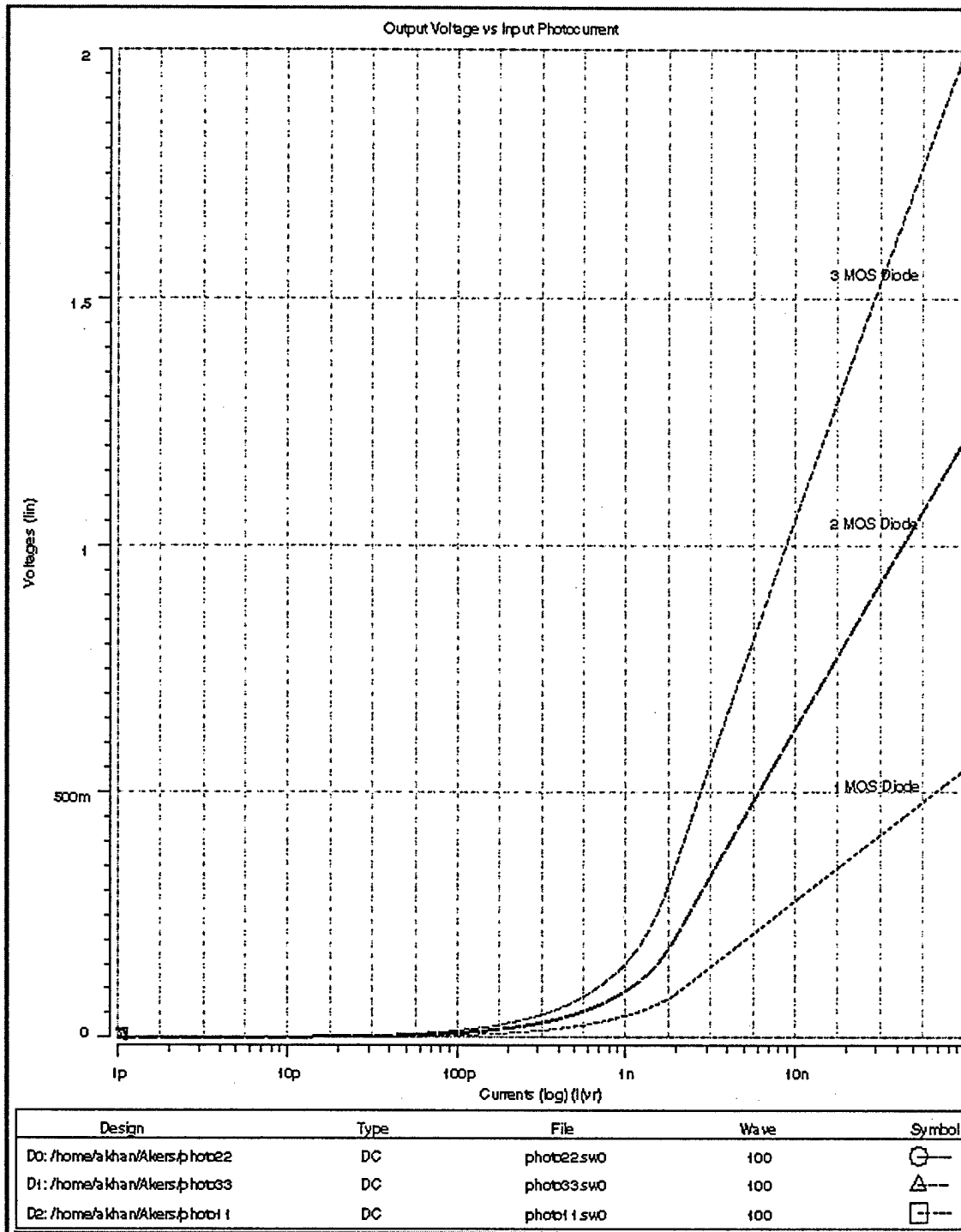


Fig. 3: Simulation Results of Logarithmic Photoreceptor Circuit

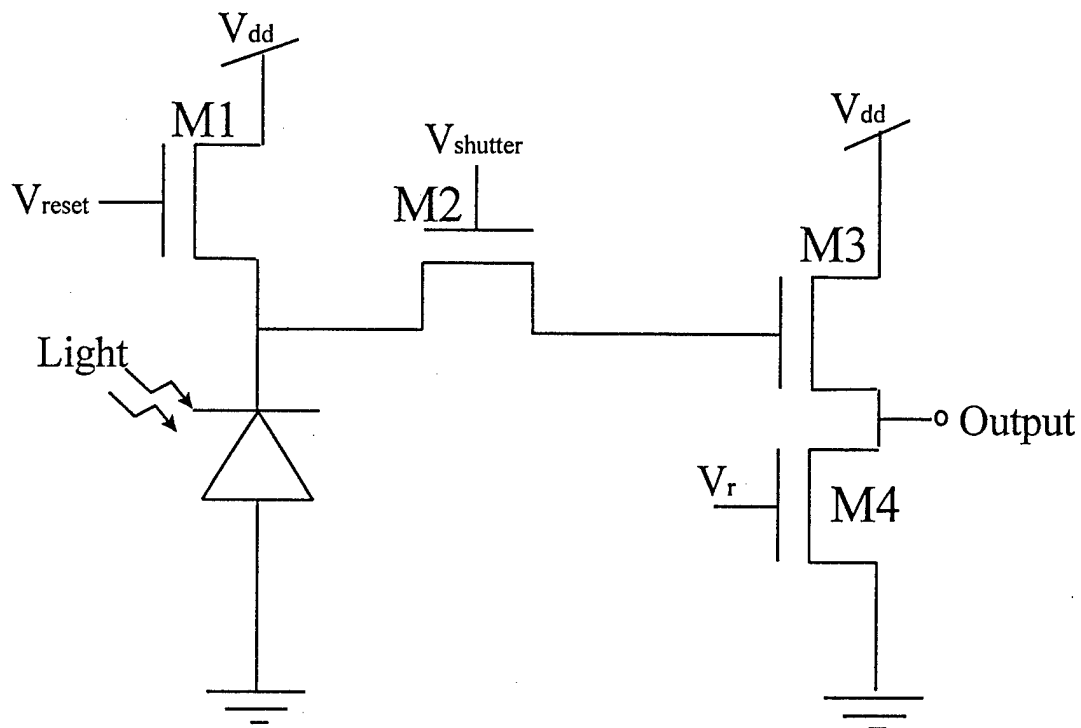


Fig. 4: Active Pixel Sensor Circuit [6]

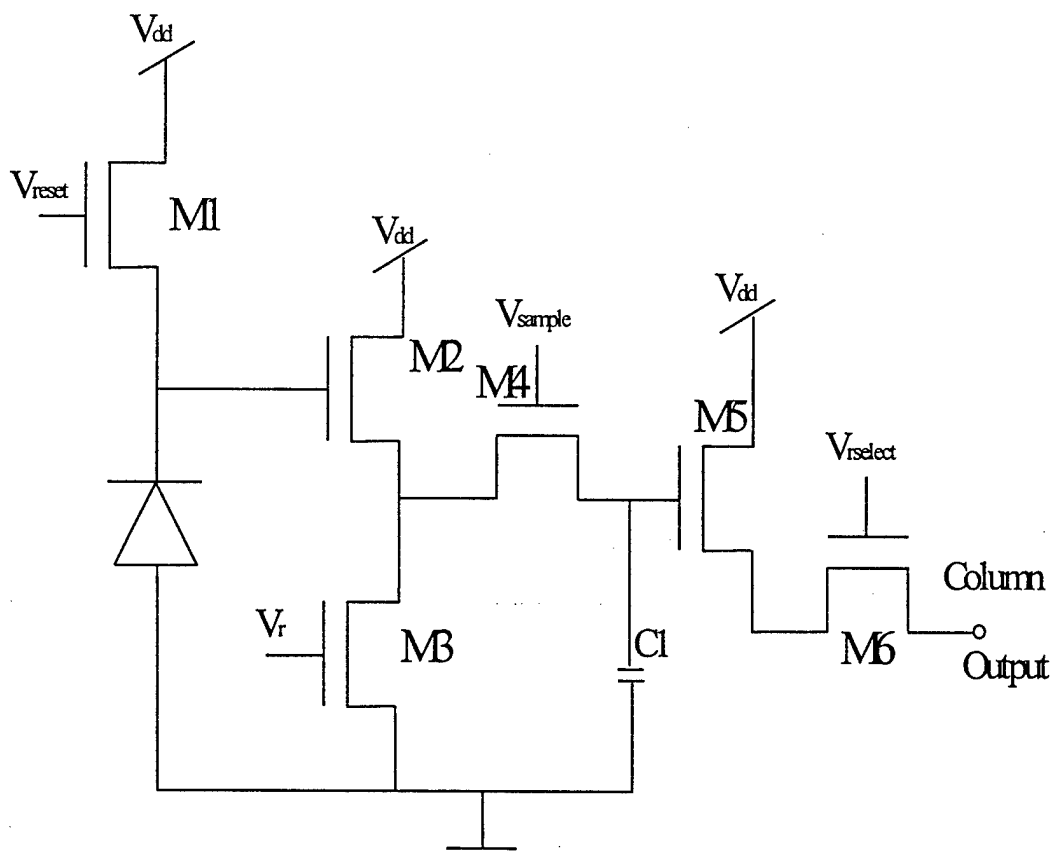


Fig. 5: Two Stage Buffer APS Circuit [7]

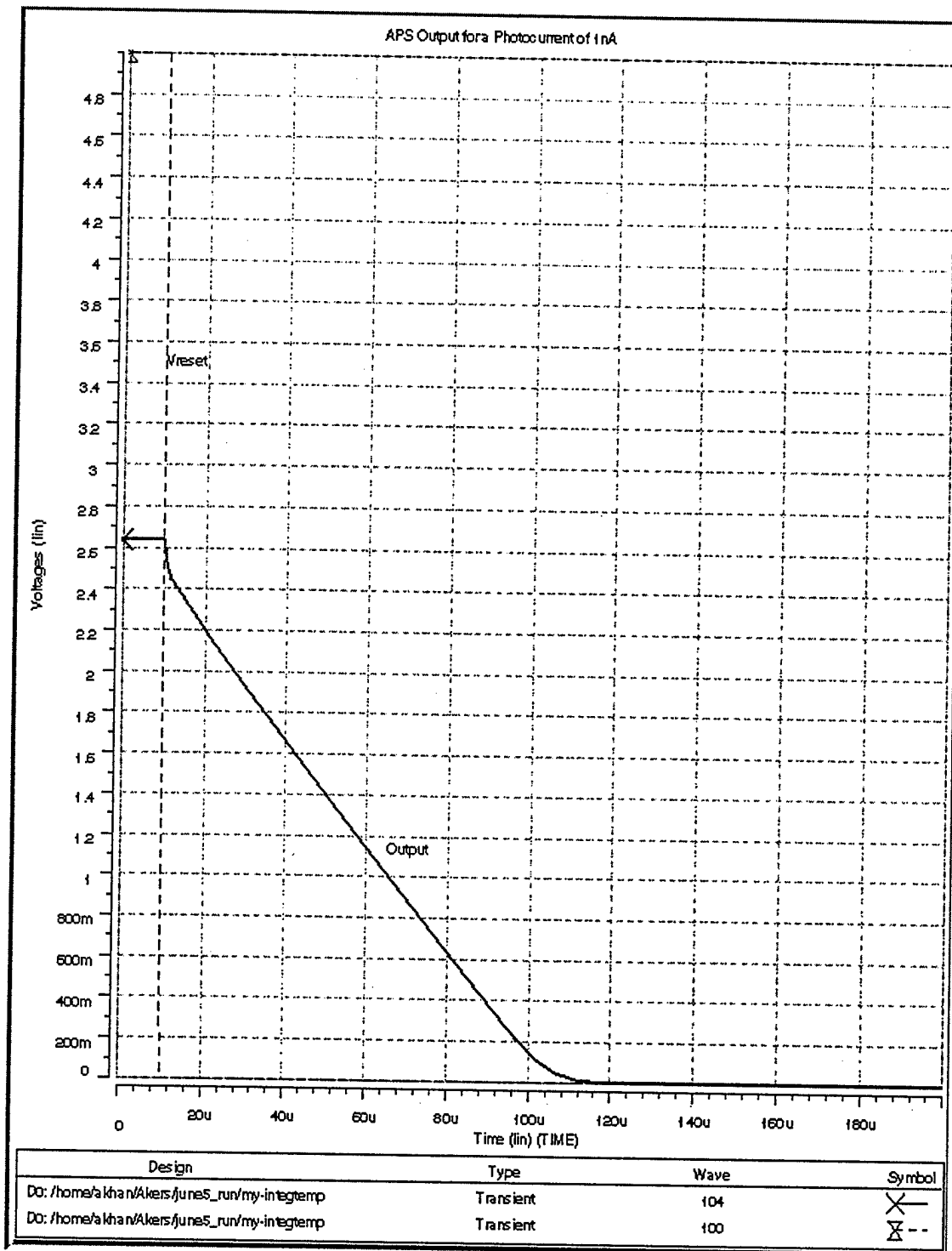


Fig. 6: Simulation Result of APS Circuit for 1nA Photocurrent

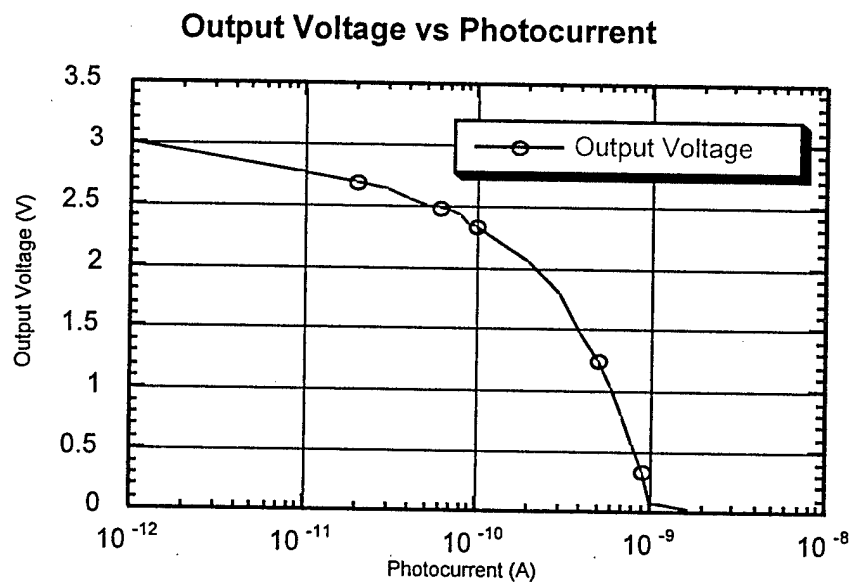


Fig. 7: Complete Simulation Results for APS Circuit

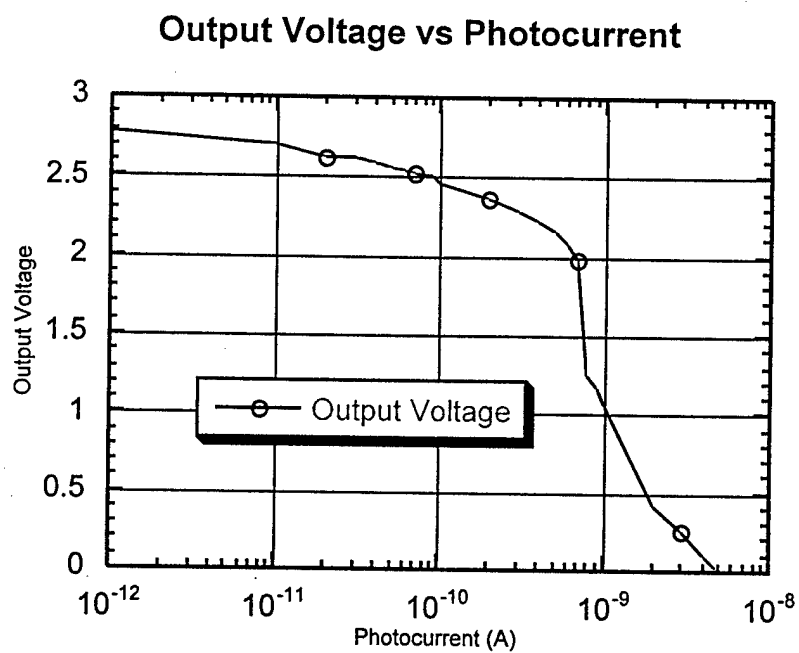
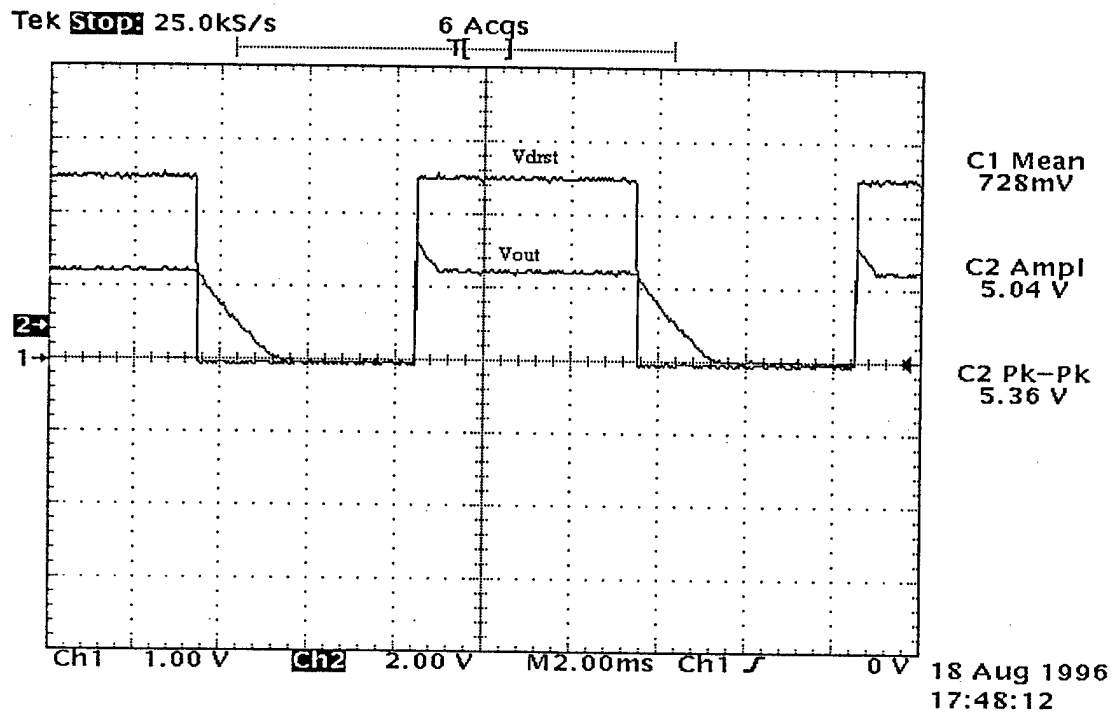
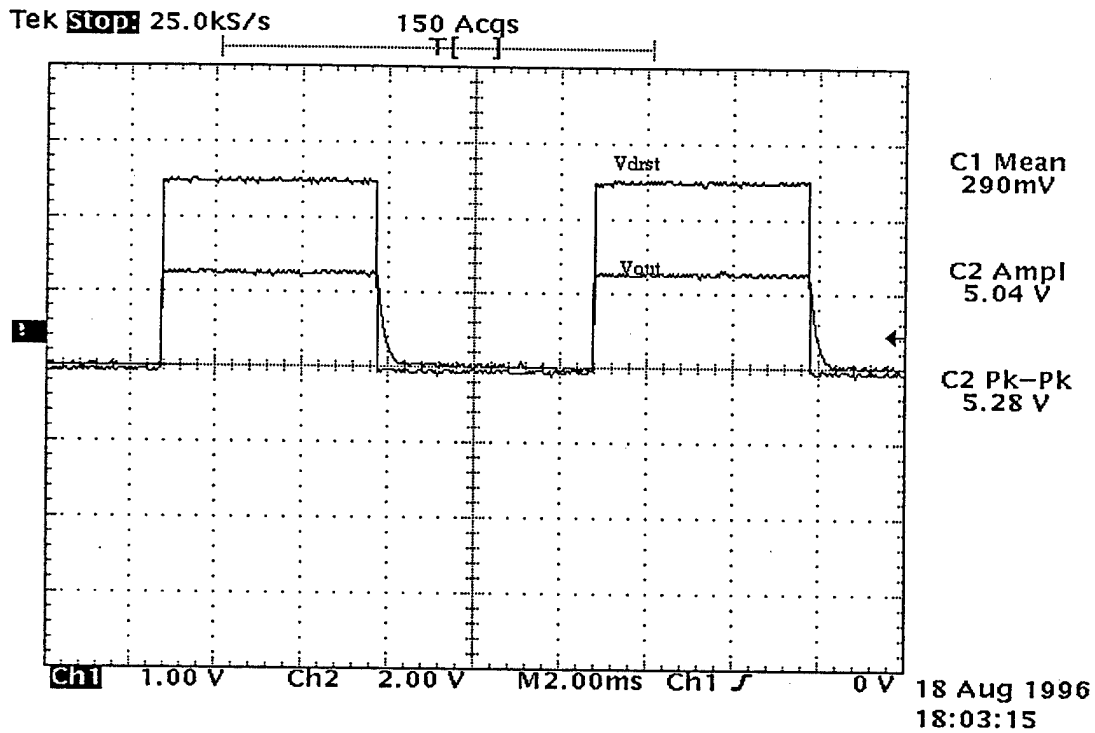


Fig. 8: Simulation Results for two Stage APS Circuit



(a) Output Voltage Response in Room Light; Ch1= Vreset Signal, Ch2 = Voutput Signal



(b) Output Voltage Response in Lamp Light of 850Lumens( $3.35\mu\text{W}$ ); Ch1= Vreset Signal, Ch2 = Voutput Signal

Fig. 9: Experimental Results for two Stage APS Circuit.

### C. Adaptive Photoreceptor Circuit

A small increase in the photocurrent,  $i$ , tries to pull down  $V_p$  by  $(i/I_{bg})V_t$ . In response  $V_o$  goes up  $A_{amp}$  times as much. The output change is coupled back to the gate of  $Q_{fb}$  through the capacitive divider. This raises the gate voltage of  $Q_{fb}$  which pulls up its source. The feedback amplifier and the input fight to control the source voltage of  $Q_{fb}$ , but the feedback amplifier wins because it has much higher gain. The feedback effect clamps  $V_p$ . The adaptive element is such that for large signal changes it behaves as a short circuit and  $V_p$  is clamped fast. While for small changes it offers large resistance and the feedback voltage is due to the capacitive divider. This circuit provides a continuous time output which is a logarithmic function of the input. The dynamic range of this circuit is 6 decades. The advantage of this circuit is that it significantly amplifies fast changes and slowly adapts to the average temporal intensity, although this implies a low output voltage swing to resolve DC changes in light intensity. Also, this circuit employs an adaptive element which takes a large area. The circuit uses an isolated well for the adaptive element and two special capacitors.

control for amplification, spatiotemporal bandpass filtering for preprocessing and adaptive sampling for quantization, all at the pixel level.

#### D. Current Mode CMOS Imager

Current mode circuits are easier for implementing some functions than voltage mode circuits. An example that can be presented is the summing operation. It is simpler to sum currents than voltages. Light intensity is directly transformed into flow of electrons/holes, and manipulation is easier with it than voltages. The photocurrent obtained at environmental illumination (bright-current) is reported to be 20nA for a photodiode of  $100\mu\text{m} \times 100\mu\text{m}$  [11]. The photocurrent is area dependent and since small photodetectors are needed, a better way to increase the strength of a signal is to use a vertical BJT detector than an amplifier which takes more area. The current generated by this device is  $\beta$  times larger than that of a photodiode with the same well area (if well-substrate photodiode was used). To further strengthen the signal a Darlington pair can also be used.

A current mode photodetector based on the notion discussed in the previous paragraph is shown in Fig. 11. This sensor gives a output which is proportional to the difference between two currents. If the concept of local adaptation is applied the current can be the average photocurrent from a group of close pixels. The output is proportional to the difference between absolute light intensity and average light intensity. This signal can be further processed to implement edge and bar detection functions. The main advantage of this kind of circuit is its good signal strength and easy processing capabilities. The disadvantage of this circuitry is due to its gain of  $\beta$  it amplifies dark current also. If a Darlington pair is used then the dark current amplification is  $\beta^2$ .

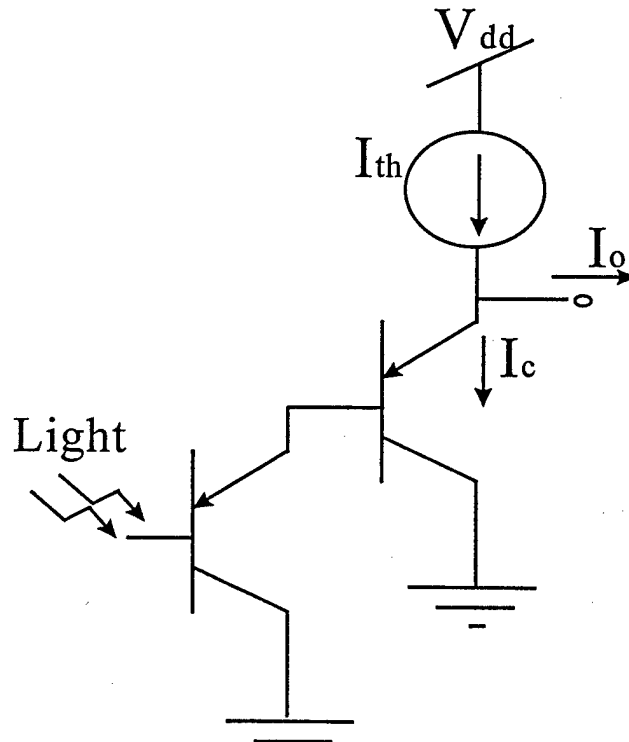


Fig. 11: Current Mode Photodetector Circuit [2]

#### E. Need for a New Circuit

The main idea that is obtained from the previous section is that an ideal photodetector is one that should have large dynamic range, high sensitivity, low noise, less dark current and most importantly it should be adaptive to the changing light intensity. The adaptation should be local and not global. Our idea is not to mimic the biological vision systems. The main aim was to develop an active pixel sensor circuit which did not compromise sensitivity for dynamic range. If the active pixel sensor could respond to the variation in light intensity by changing its gain, in other words the APS could adapt to the light intensity, then it would have better dynamic range and sensitivity.

### III. Locally Adaptive Multimode Photodetector

We present a circuit that is an active pixel sensor, is locally adaptive and operated with more than one level of gain automatically determined by the local light level. The notion of this circuit is based on the CMOS photodetector proposed by Ward et. al[2]. However, Ward's circuit did not contain the circuitry to automatically switch the gain depending on the local light level. The photodetectors presented till now used a photodiode or phototransistor, both featuring a single mode of operation. A drawback with photodiode is that it is relatively insensitive to light with less intensity, and consequently large areas are required. A phototransistor can be implemented in approximately the same area (compared to a well-substrate photodiode) which is more sensitive to detect an optical signal that is weak [2]. However, the drawback with this approach is it consumes more power and amplifies the dark current. A detector that can combine the good qualities of both is one that can be operated as a phototransistor for low light levels and then as a photodiode in higher light levels. The main idea behind this photodetector is to divide the range of light intensity into two regions and operate the circuit in these two regions. The sensitivity of the detector increases by operating the detector circuit in these two modes. The output of this photodetector circuit is the output voltage and the region of operation.

The vertical bipolar junction transistor and pn diode in a CMOS process share identical structures with n-well being the base of either vertical pnp transistor or a diode. The diode can be the n-well and p-substrate or p-diffusion and n-well. This two mode detector is a phototransistor with a MOSFET connected between its emitter and base. When the structure is operating as a photodiode, the output signal can be taken from either of the two pn junctions present in the device. The photocurrent from the p-substrate to the n-well can form one output signal, and the photocurrent from the p-diffusion to the n-well can form the other. When the device is operating as a phototransistor, the p-substrate forms the collector (which is grounded in a n-well process), the n-well is left floating to form the base, and the output is taken from the p-diffusion emitter.

The use of a MOSFET can force this device into one of the two modes described above. The MOSFET acts like a switch and either a PMOS or a NMOS can be used. As shown in Fig. 12, the MOSFET is connected between the base-emitter junction. In the diode mode, the MOSFET is turned on and permits the substrate to n-well photocurrent to flow directly to the p-diffusion emitter, so no transistor action occurs. The resulting output is simply due to the light falling on the reverse-biased p-substrate to n-well junction. When the MOSFET is turned off, electron/hole pairs generated by photons adds to the base current of the vertical transistor which is amplified by the forward current gain  $\beta$  of the device. Thus the collector current which is approximately equal to the emitter current (output) is  $\beta$  times the original photocurrent of the photodiode. The value of  $\beta$  is a process dependent parameter and varies from 10-100 [13]. Further modes can be achieved with two transistors connected as a Darlington pair and with the use of MOSFET switches they can be switched into different modes depending on the light intensity. Figure 13 shows such a structure.

The dark current is an important issue since it also get amplified by  $\beta$  when in the phototransistor mode. If a Darlington pair structure is used then it is amplified by  $\beta^2$ . The typical value of dark current is 1pA/cm[14]. We cannot detect an optical signal whose response photocurrent is equivalent or less than the dark current of the device. The Darlington pair was not used because of the large dark current and also since the two modes are enough to cover the light intensity range in which we are interested.

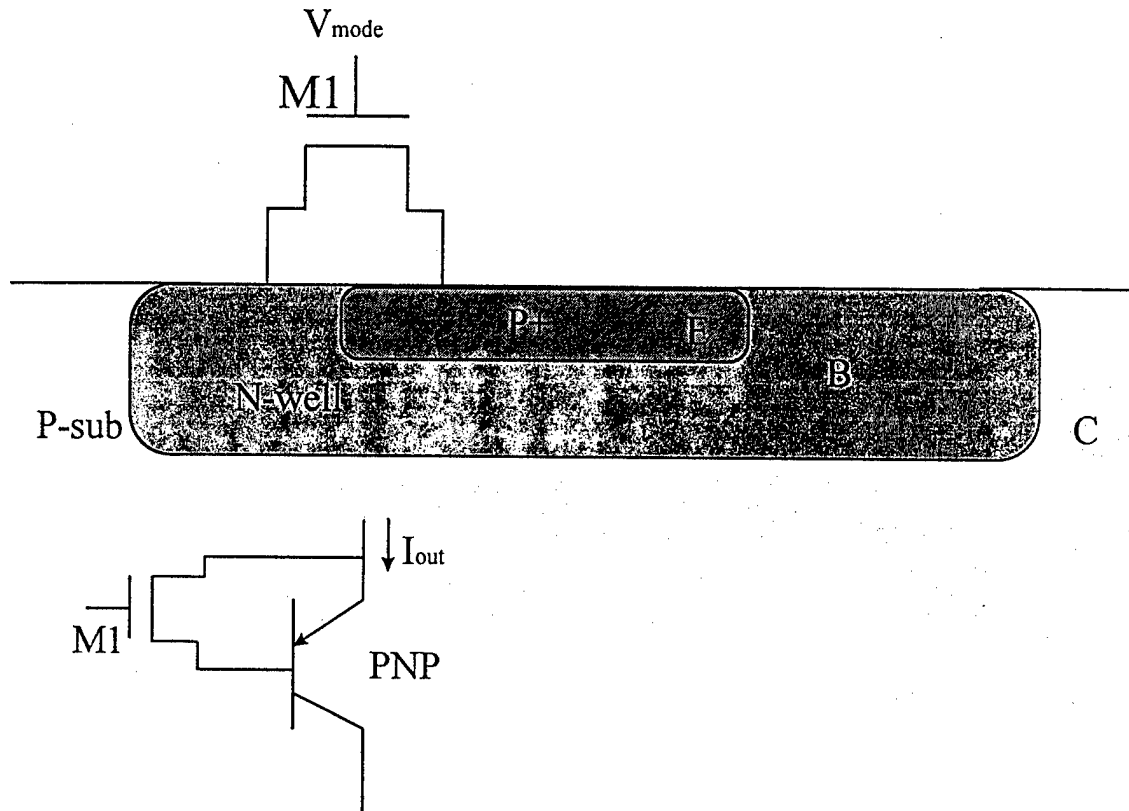


Fig. 12: Multimode Photodetecting Element

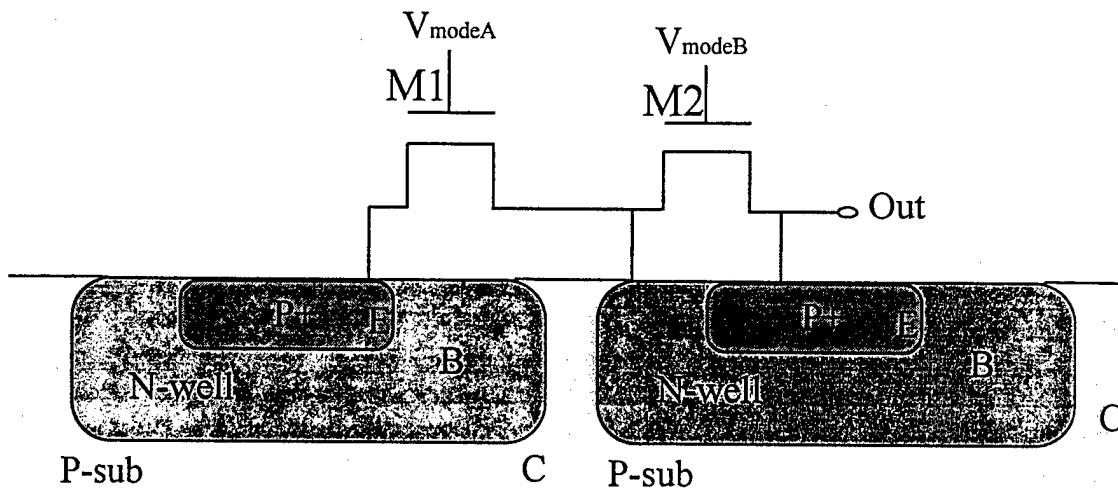


Fig. 13: Darlington Pair Mode Photodetecting Element

The notion of the multimode photodetector is based on the principle of local adaptation. The light intensity varies over a wide range and we need a circuit that adapts itself to this wide range maintaining its sensitivity. The idea is to divide an array of photodetectors into cells and each cell can comprise of 4 photodetectors [12]. The number of photodetectors per each cell depends on the layout and routing constraints. If 4 photodetectors are used per cell then it is easy to replicate and route them. A cell of four detectors consists of a controlling circuitry and this controls the mode of operation of all the detectors in a cell. The photodetectors adapt automatically to the changing light intensity under the direction of the

control circuitry. The assumption made in designing this circuitry is that we would be able to achieve sufficient density of pixels on the chip, so the light intensity will change gradually from one pixel to another.

The multimode photodetector circuit that will be placed in a cell at each pixel consists of a multimode photodetector element, a shutter transistor, a reset transistor and an optional source follower transistor. The circuit diagram is shown in Fig. 14. The circuit is based on the principle of charging a node to  $V_{dd}$  and then discharging it with a current proportional to the light intensity, in a fixed time period. The time period is controlled by the shutter transistor M2. The time period is usually in the range of  $\mu\text{Sec}$ . The node is reset to  $V_{dd}$  by the reset transistor M3 in every cycle. The swing of this circuit is nearly 5V. Transistor M1 switches the detector into different modes.

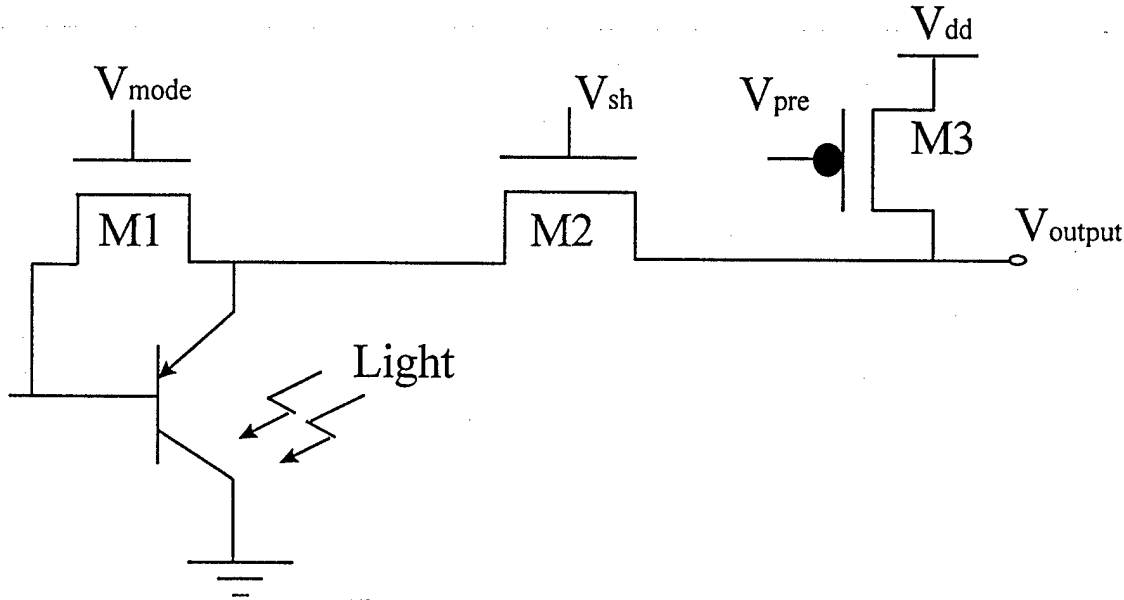


Fig. 14: Multimode Photodetector Circuit

When the light intensity is less, the corresponding photocurrent is so low that it requires time in seconds to appreciably discharge the reset node voltage, then we need some kind of mechanism to amplify the photocurrent. The transistor M1 is switched off during low light levels and the photocurrent gets amplified by  $\beta$  and this resulting current appreciably discharges the reset node voltage. When the light intensity is more, M1 is switched on so that it shorts the emitter-base nodes so that no transistor action takes place. The photocurrent during this time is enough to substantially discharge the reset node. An important consideration is the fixing of threshold photocurrent at which the switching of the mode is done. This threshold is obtained from simulations. A significant observation from the simulations of a photodetector consisting of a photodiode is that, in a fixed discharge time, the photocurrent output vs voltage plot has a parabolic shape.. This causes a problem in fixing the threshold level for switching because the  $V_{ref}$  to be fixed is compared with an output voltage from the photodiode in the control circuitry and this voltage does not change substantially in the lower light intensity.

The control circuit consist of a photodiode, and PMOS comparator circuit with a inverter at the output. Figure 15 shows the circuit diagram. The photodiode is basically used to give the information about the region of operation. The layout is done such that this photodiode sits in the middle of the cell. The assumption made is that the light falling on this diode is approximately the same as that falling on all the four pixels and the photocurrent obtained from this is the average photocurrent of the cell. The output of the photodiode (node Z1) is given to a comparator that compares the voltage corresponding to the average photocurrent, to a fixed reference voltage( $V_{ref}$ ). If the voltage obtained is less than  $V_{ref} - V_{th}$  then transistor M14 switches on resulting in the switching on of transistor M10 also. When M10 turns on node Z2 goes to '0' and this value is sampled to the inverter whose output will be 1. The output of the inverter is given to the transistor M1 of Fig. 14.

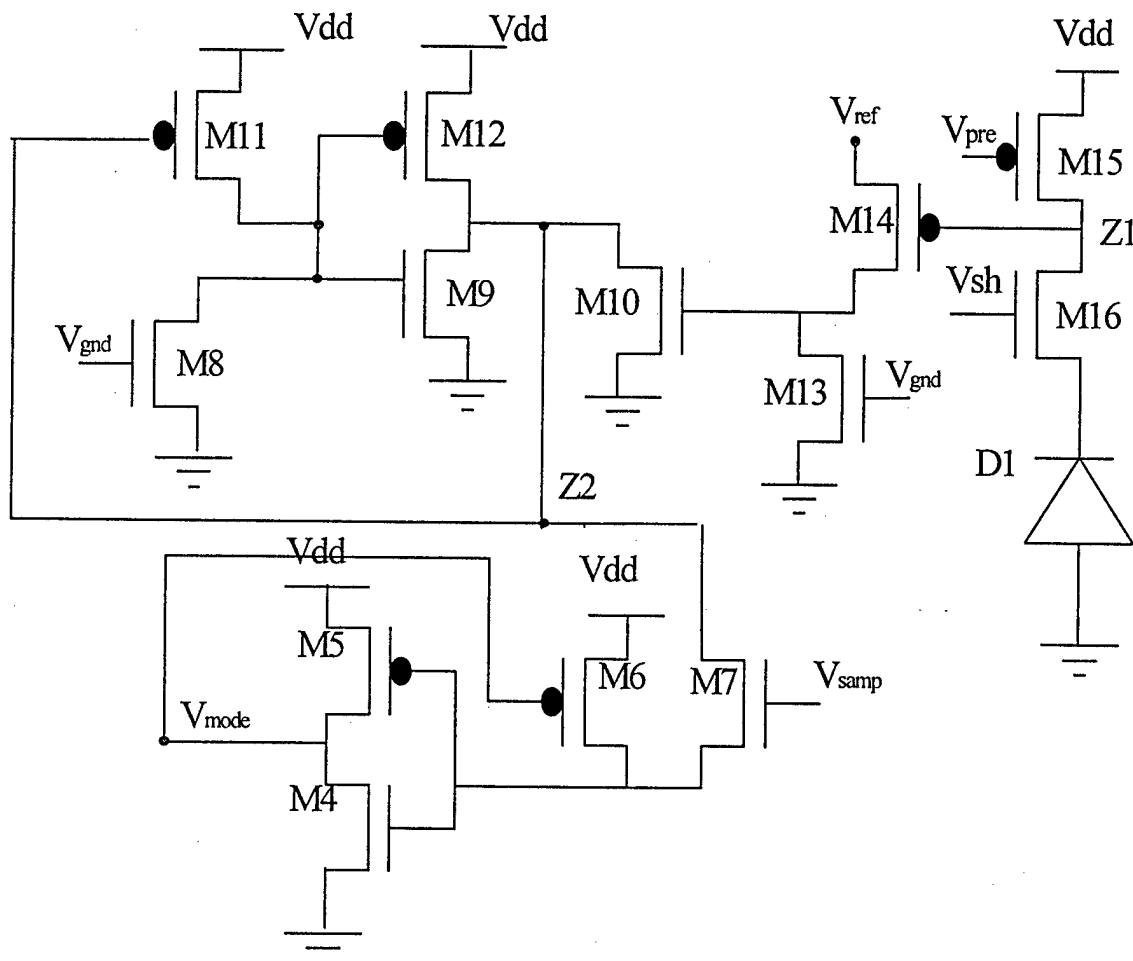


Fig. 15: Control Circuit For Multimode Photodetector Circuit

The '1' indicates that the light intensity is in the brighter region and the multimode photodetector should operate in the diode mode. The diode mode is selected by turning on the M1. If the light intensity is less and the voltage at Z1 is greater than  $V_{ref}$  then M14 remains off and the node Z2 is high due to the precharge signals  $V_{gnd}$ . When this high is sampled to the inverter then the gate voltage of M1 ( $V_{mode}$ ) is 0 signifying the BJT mode. The multimode photodetector is operated in two modes, diode mode and transistor mode. Transistor M1 controls the mode of the circuit, depending on the light intensity. If  $V_{mode} = 1$  then it operates in the diode mode,  $V_{mode} = 0$  corresponds to the BJT mode. The timing of the input control signals is shown in Fig. 16. The mode selection is done automatically, and the output of the pixel is a 1 bit  $V_{mode}$  signal and the value of  $V_{output}$  which can be encoded in 7 bits. Thus the output can be encoded into an 8 bit signal.

The circuit was simulated with HSPICE using the Orbit's  $2\mu$  CMOS process parameters. For simulation the value of photocurrent was substituted in place of the reverse current  $I_s$  in a BJT .MODEL parameters. Using the timing shown in Fig. 16, simulation results of the circuit are shown in Fig. 17. The circuit starts in the BJT mode and as the photocurrent is increased, after some point (500pa), it shifts into the diode mode. The point at which the switch from BJT mode to diode mode, takes place is determined by the voltage  $V_{ref}$  and shutter time  $T_{sh}$  which were fixed with simulation.

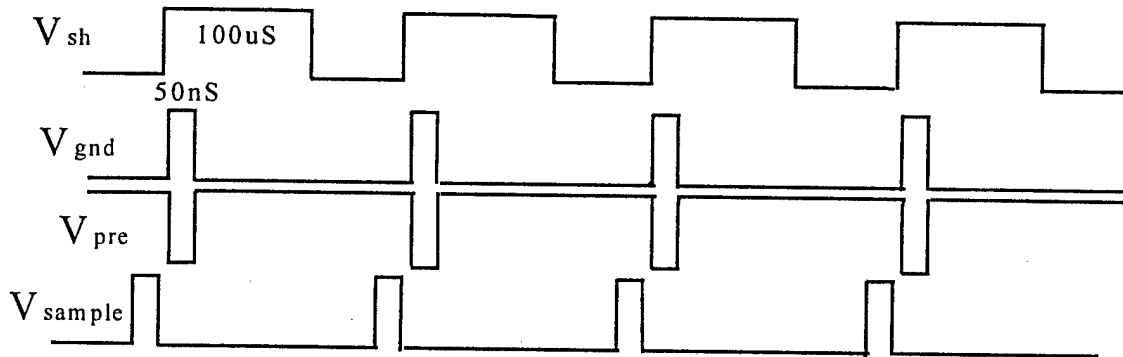


Fig. 16: Timing Diagram for Locally Adaptive Multimode Photodetector Circuit

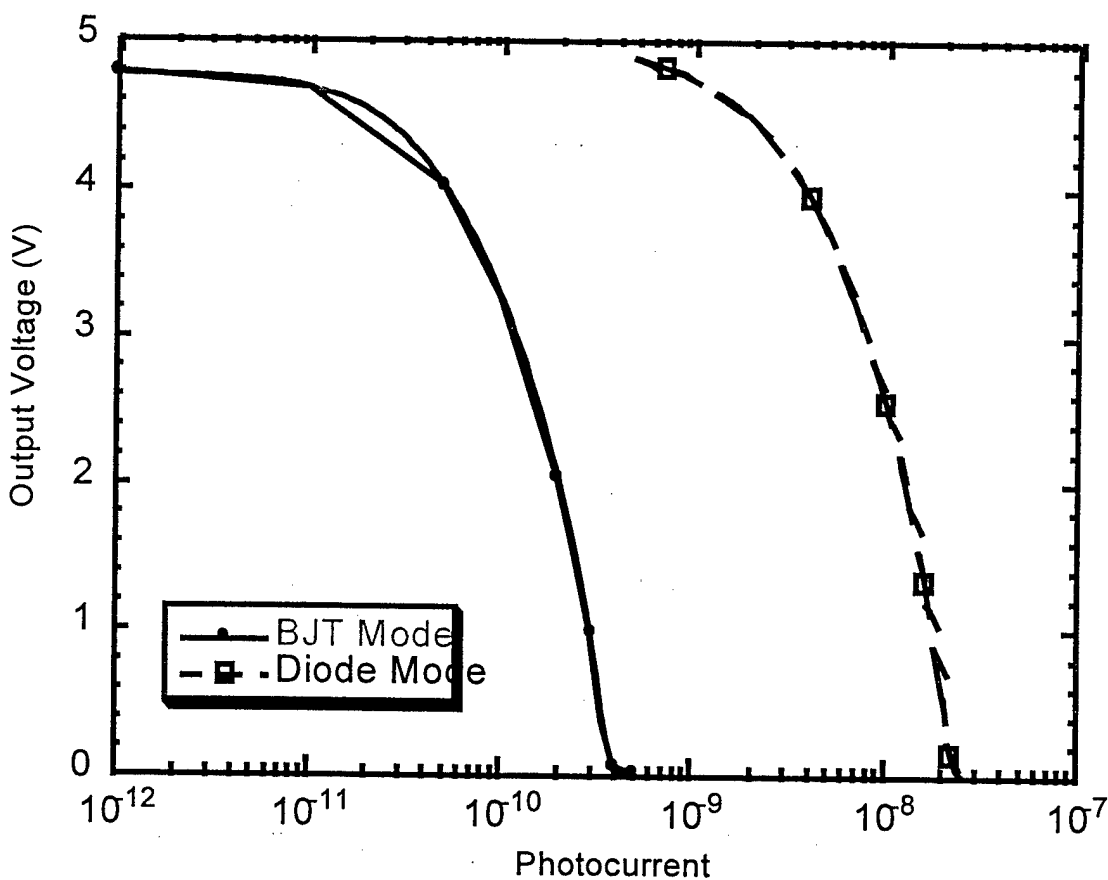


Fig. 17: Simulation Results of Locally Adaptive Multimode Photodetector Circuit. The Curve Fits are also shown.

## IV. Experimental Results

The circuit was designed and fabricated in the 2 $\mu$ m CMOS process through MOSIS. Figure 18 gives the experimental results of this circuit. In these figures CH1 is the precharge signal, CH2 is the shutter pulse and CH3 is the output voltage. The output was verified for three different light levels and the results are as expected from the simulation graphs. Figure 18(a) gives the output voltage discharge in the diode mode for the lamp light. When this is compared with Fig. 18(b), which give the response of the detector in the BJT mode for the same light level, it can be seen that discharge rate is more for the BJT mode than the diode mode. The three different light sources were the light of approximately 850 lumens from a 100W bulb, room light and darkness of the lab. In the darkness we get to see the effect of the dark

current Figures 18(c) and (d) show the diode and BJT circuits at room light with a shutter speed of 10 $\mu$ s. Again, as expected the BJT circuit discharges faster. The effect of dark current is shown in Figs. 18(e) and (f).

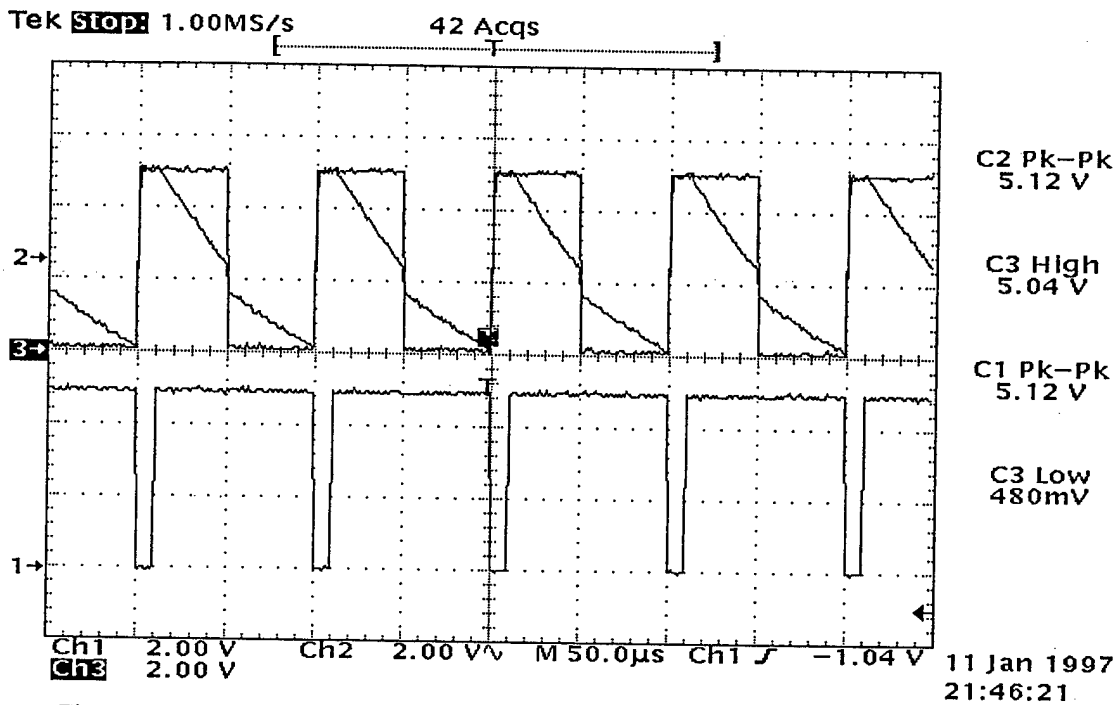


Fig. 18(a) Diode Mode in Lamp Light; Ch1=Vpre Signal, Ch2=Vsh Signal, Ch3=Voutput Signal

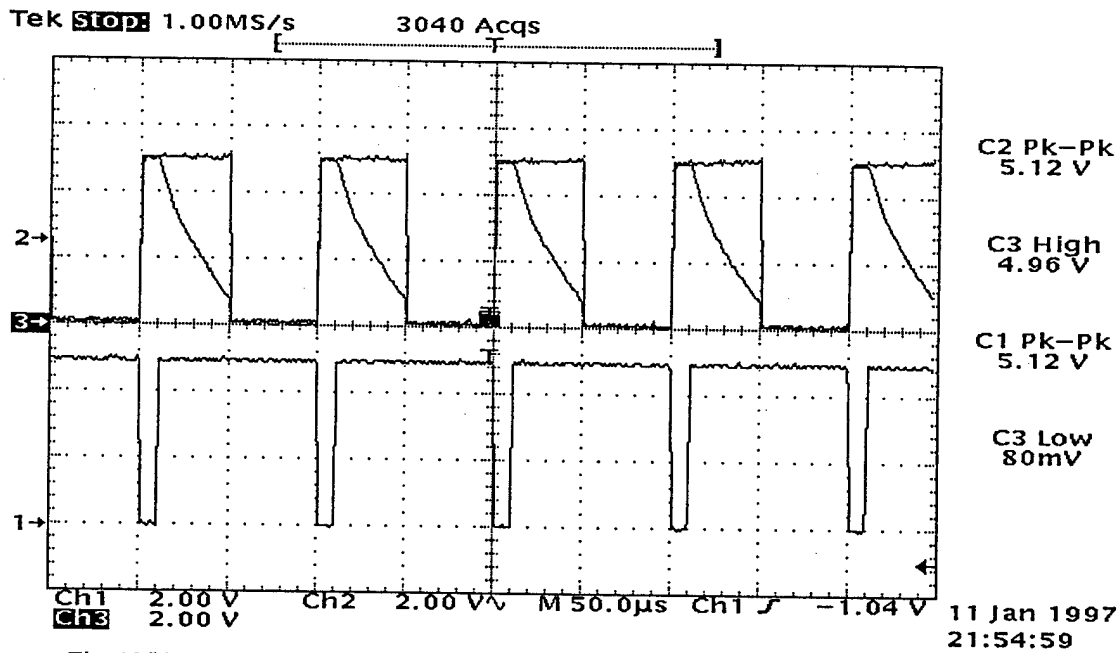


Fig. 18(b) BJT Mode in Lamp Light; Ch1=Vpre Signal, Ch2=Vsh Signal, Ch3=Voutput Signal

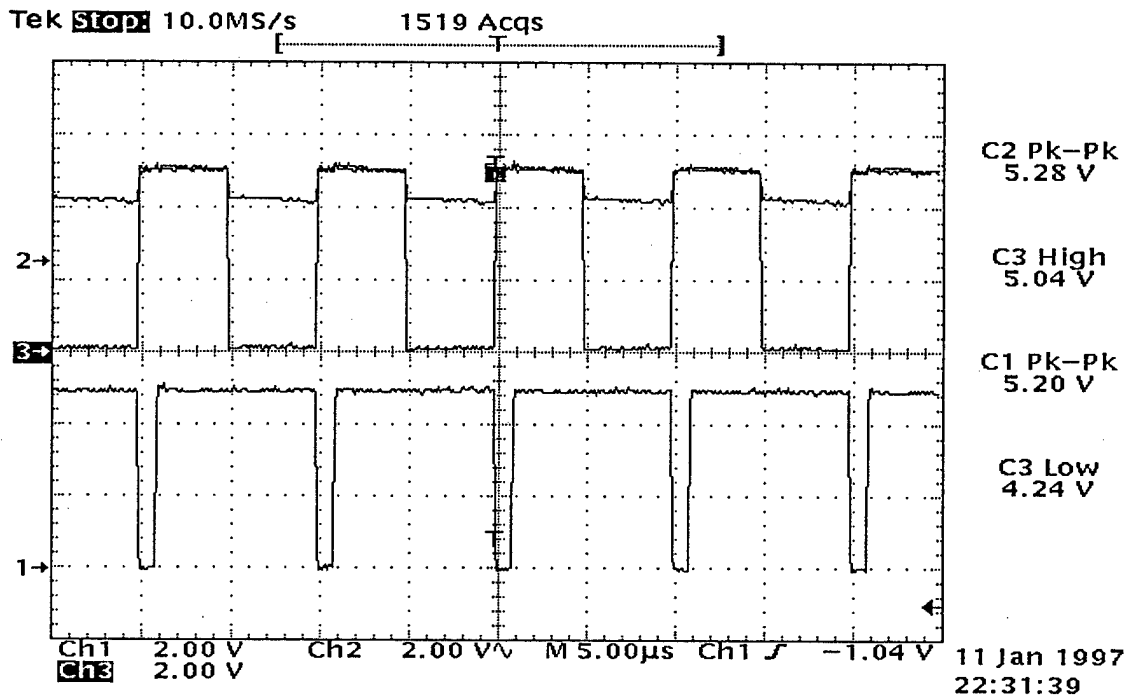


Fig. 18(c) Diode Mode in Room Light for 100KHZ Frequency(10us); Ch1=Vpre Signal, Ch2=Vsh Signal, Ch3=Voutput Signal

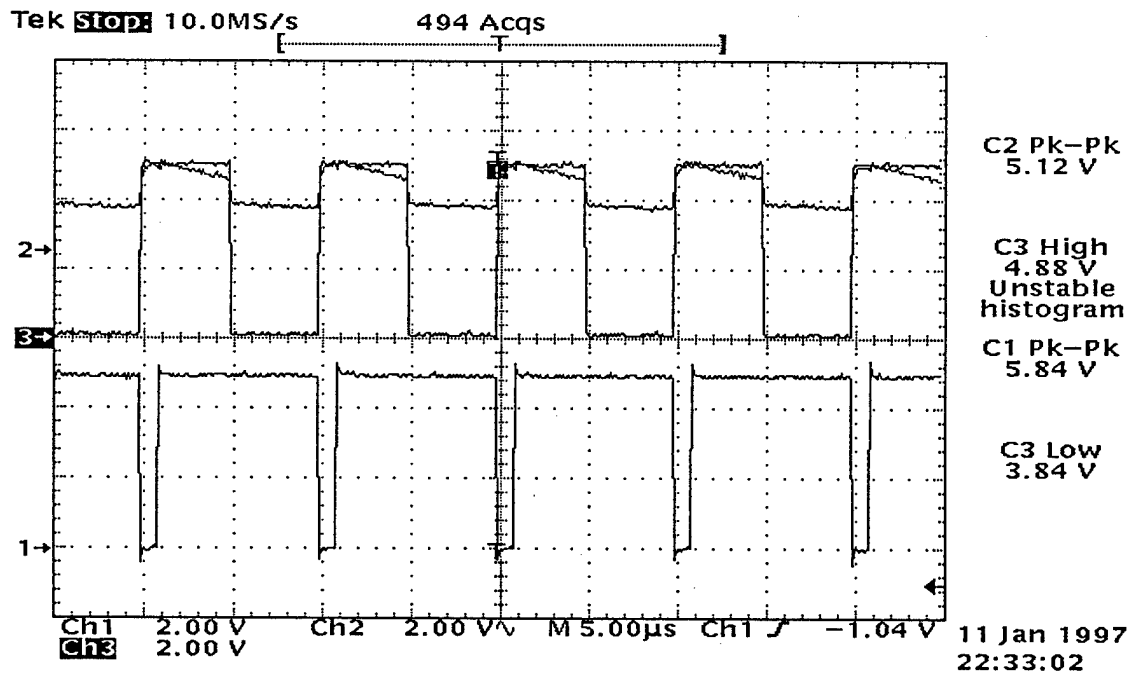


Fig. 18(d) BJT Mode in Room Light for 100KHZ Frequency(10us); Ch1=Vpre Signal, Ch2=Vsh Signal, Ch3=Voutput Signal

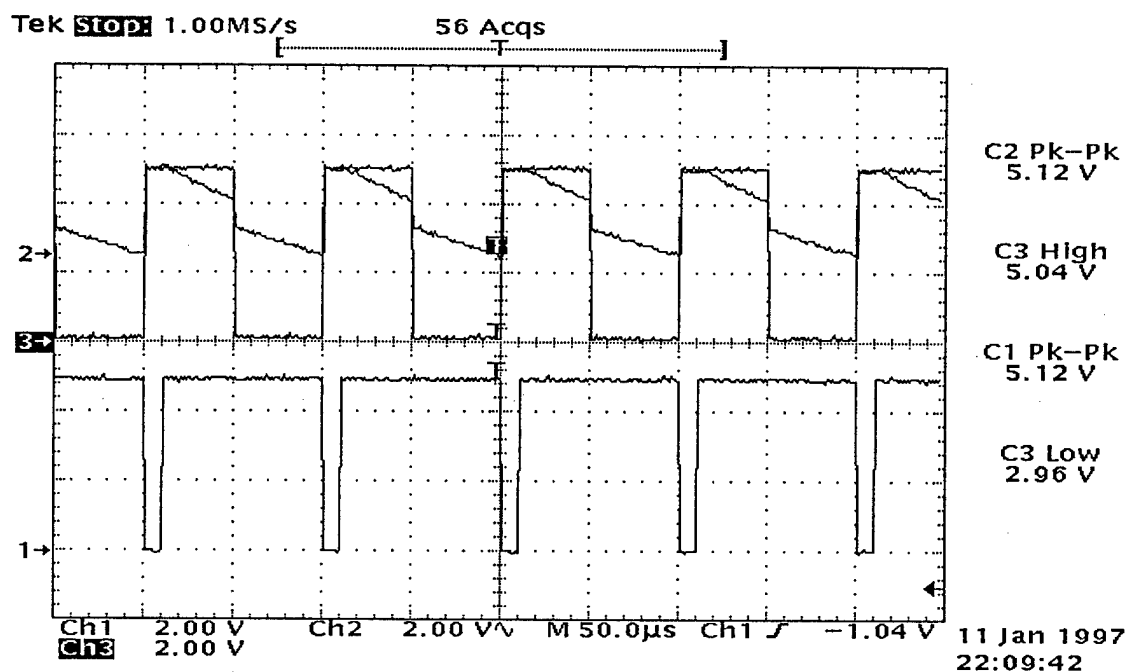


Fig. 18(e) Diode Mode in Dark; Ch1=Vpre Signal, Ch2=Vsh Signal, Ch3=Voutput Signal

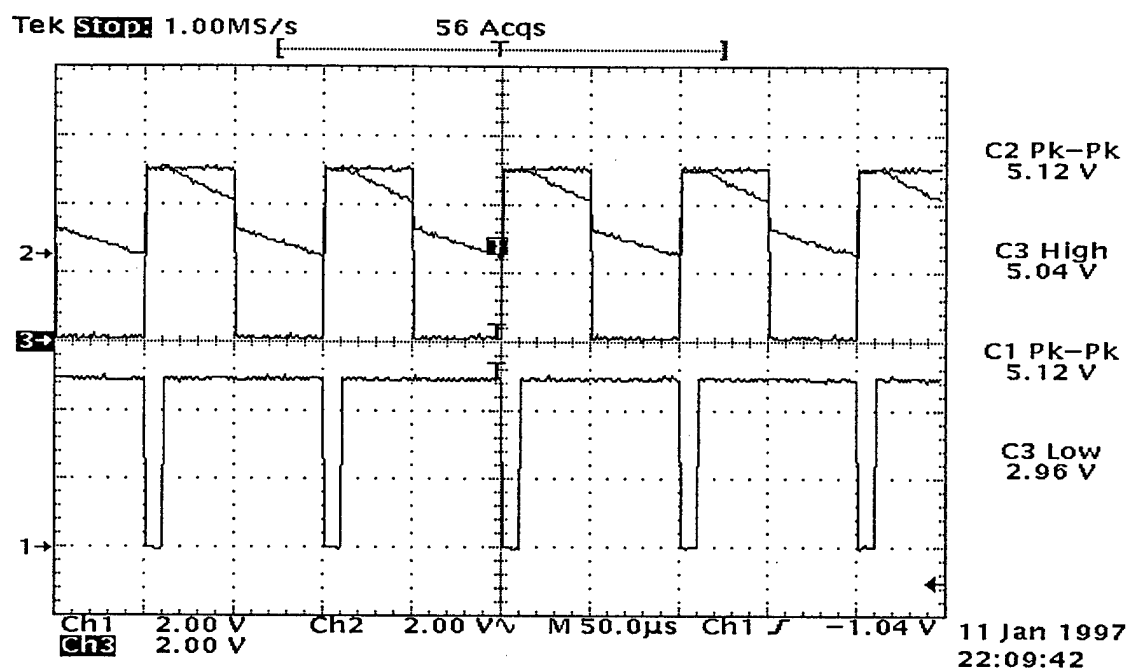


Fig. 18(f) BJT Mode in Dark; Ch=Vpre Signal, Ch2=Vsh Signal, Ch3=Voutput Signal

Fig. 18 Experimental Results for Multimode Photodetector Circuit

Figure 19 gives the experimental results for changing light conditions. The important observation from these figures is that the mode (CH4) changes from 0→1 automatically with an increase in light intensity. Figure 19(a) gives the output voltage response (CH3) for BJT mode since the light intensity is due to room light only. When the intensity is increased by turning on the lamp, the circuit shifts

automatically into the diode mode, as shown in Fig. 19(b), and the output has discharged to nearly the same voltage as before, though it's at higher intensity. The output discharges for a time shown by CH1.

Layout considerations are important, since we have assumed that light intensity is going to be nearly the same over a particular cell. The cell should be small enough such that we get high density of pixels in the array and our assumption holds. The mode control circuitry with the diode detector should be placed in the center of the cell. This placement is done for the diode detector to receive the average light intensity. One dimension of the photodetecting cell is 20 times the minimum feature size of the process technology used. The photocurrent through a photodiode is proportional to its area and due to this, the area of the photodiode in the control circuitry 'D1' is the same as the base area of the phototransistor. The base-collector junction of the phototransistor behave as the photodiode, during its diode mode. The layout for these circuits was done for the  $2\mu\text{m}$  CMOS process, therefore the size of the photodiode was selected to be as  $40\mu\text{m} \times 40\mu\text{m}$ . The photodiode used is a diffusion-substrate junction diode and the phototransistor is a vertical diffusion-well-substrate parasitic pnp transistor. The emitter area in the n-well base was sized according to the design rules, i.e. it was as large as allowed by the design rules. The fill factor is also important issue in the array of pixels, and with this cell of 4 pixels a fill factor of approximately 20% was obtained. The non-photoactive regions are covered with metal2 layer to prevent the effect of light on the operation of the other transistors. This allows us only metal1 and poly for local interconnection. Guard rings have also been put for anti-blooming protection. These guard rings also reduces the effect of cross talk [7].

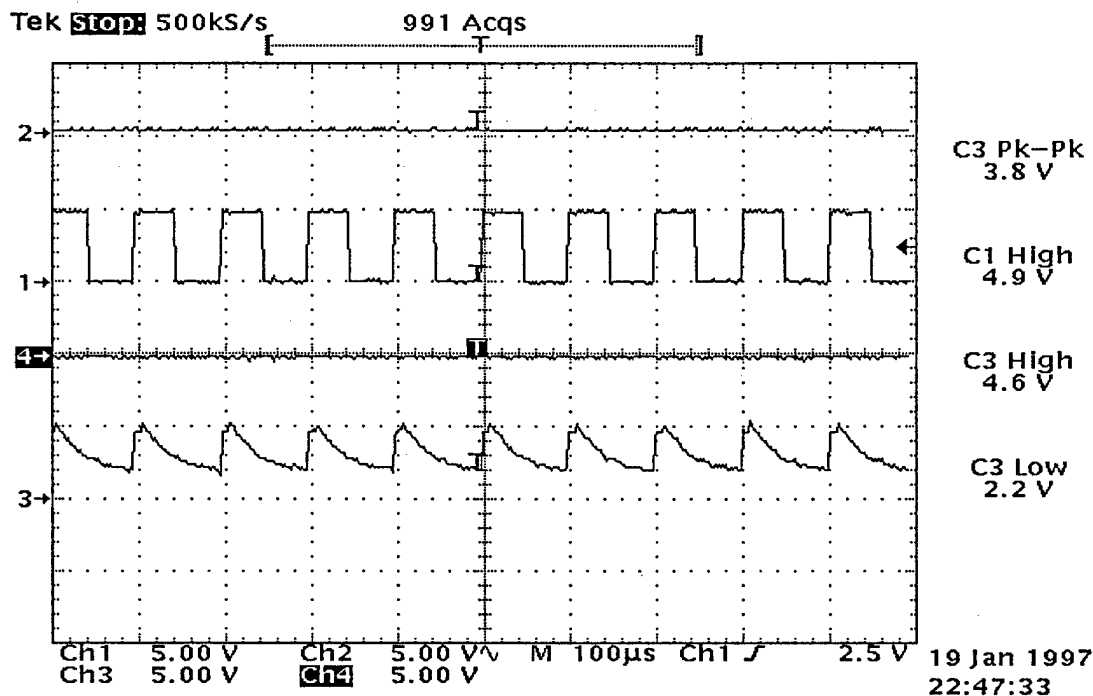


Fig. 19(a) BJT Mode in Room Light for  $V_{\text{ref}}=3\text{V}$ ; Ch1= $V_{\text{sh}}$  Signal, Ch3= $V_{\text{output}}$  Signal, Ch4= $V_{\text{mode}}$  Signal

It is important to discuss the advantages and disadvantages of the locally adaptive multimode photodetector circuit. As stated earlier the main advantage of this circuit is its excellent sensitivity over large dynamic range. The dynamic range of the circuit is also comparable to the other circuits. The dynamic range of this circuit is calculated as approximately 95dB. The other advantage of this circuit is the scheme is cellular based and it implements local adaptation instead of global adaptation. The drawback of this circuit is its large dark current due to the transistor action which can be observed from the experimental results. Due to the limitation of the testing equipment, the leakage of current in a oscilloscope is comparable to the dark current and we do not observe significant change in voltage for different modes in the dark. This has the effect of reducing the dynamic range, but the range achieved with this circuit is comparable to existing

circuits. Another drawback is its less fill factor, but with clever layout techniques this could be improved. The other problems of this circuit are similar to the ones suffered by other circuits such as fixed pattern noise, scaling problem, blooming, lag etc. General techniques such as correlated double sampling, uniform doping, etc. can be used to reduce these effects for this circuit also.

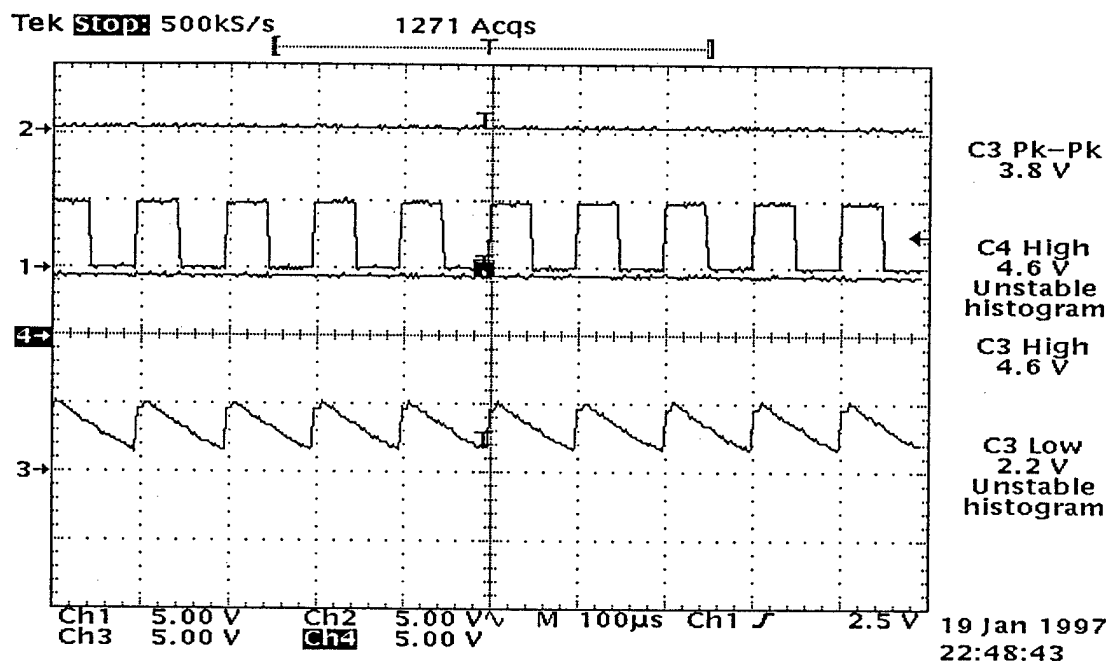


Fig.19 (b)Diode mode in Lamp Light for  $V_{ref} = 3V$ ; Ch1= $V_{sh}$  Signal, Ch3= $V_{out}$  Signal, Ch4= $V_{mode}$  Signal

Fig. 19 Experimental Results for Locally Adaptive Multimode Photodetector Circuit

## V. Summary

We have given a description of the design and measurement of the locally adaptive multimode photodetector circuit. Simulation supported with the hardware results were presented. The advantages and drawbacks of this circuit were also brought out. This circuit can be used in applications where light intensity is varying locally over large orders of magnitude and sensitivity is a crucial factor.

## VI. References

- [1] Fossum, E. R., "Active Pixel Sensors challenge CCDs," Laser Focus World, pp. 83-87, 1993.
- [2] Ward, V., M. Syrzycki, G. Chapman, "CMOS Photodetector with Built in Light Mechanism," Microelectronics Journal, vol. 24, pp. 547-553, 1993.
- [3] Delbruck, T., C. Mead, "Phototransduction by Continuous Time, Adaptive, Logarithmic Photoreceptor Circuits," Tech. Rep., California Institute of Technology, Pasadena California 91125, 1994.  
URL: <http://www.pcmp.caltech.edu/anaprose/tobi/recep>
- [4] Vision Chips Web site, URL: <http://www.eleceng.adelaide.edu.au/Groups/GAAS/Bugeye/visionchips/>
- [5] Mahowald, M. A., "Silicon Retina with Adaptive Photodetector," Proc. SPIE, Visual Information Processing from Neurons to Chips, Vol. 1473, pp. 52-58, 1991.
- [6] Nixon, R., S.E Kemeny, C.O Staller, E.R Fossum, "256X256 CMOS Active Pixel Sensor Camera on a Chip," ISSCC '96, pp. 178-179, Feb. 1996.
- [7] Pecht, O. Y., R.Ginosar, "A Random Access Photodiode Array for Intelligent Image Capture," IEEE transactions on electron devices, vol. 38, no. 8, pp. 1772-1779, Aug. 1991.

- [8] Boahen, K.A, A.G Andreou, "A Contrast Sensitive Silicon Retina with Reciprocal Synapses," Advances in Neural Information Processing , vol.4 pp. 762-772, 1992.
- [9] Moini, A., A. Bouzerdoun, "A Current Mode Implementation of shunting Inhibition," ICNN '97 (accepted).
- [10] Boahen K., "Retinomorphic Vision Systems I: Pixel Design," Physics of computation Laboratory, California Institute of Technology, MS 136-93, Pasadena, CA 91125.
- [11] Espejo, S., A. R. Vazquez, R. D. Castro, J. L. Huertas, E. S. Sinencio, "Smart-Pixel Cellular Neural Networks in Analog Current-Mode CMOS Technology," IEEE journal of solid state circuits, vol. 29, no. 8, pp. 895-904, Aug. 1994.
- [12] Fowler, B., "CMOS Area Image Sensors with Pixel level A/D conversion," Ph.D. Dissertation, October 1995. URL: <http://www.isl.stanford.edu/people/fowler/thesis2.ps.gz>
- [13] Weste, N.H.E., K. Eshraghian, "Principles of CMOS VLSI Design: A Systems Perspective", 2<sup>nd</sup>ed., Addison Wesley, Reading, Massachusetts, 1993.
- [14] Wong, H., "Technology and Device Scaling Considerations for CMOS Imagers," Solid State Circuits Technology Workshop on CMOS Imaging Technology, San Francisco, CA, Feb. 1996.